IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application	:	Petrus Maria De Greef
For	:	DISPLAYING ON A MATRIX DISPLAY
Serial No.	:	10/587,604
Filed	:	July 27, 2006
Art Unit	:	2628
Examiner	:	Edward Martello
Atty. Docket	:	NL040106US1
Confirmation No.	:	3561

REPLY BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Customer No.
65913

Sir:

The following remarks are directed to the points of argument raised in the Examiner's Answer mailed November 11, 2009.

I. STATUS OF CLAIMS

Claims 1-11 are on appeal.

Claims 1-11 are pending.

No claims are allowed.

Claims 1-11 are rejected.

No claims are canceled.

II. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The following grounds of rejection are presented for review:

A. Claims 1-8 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over European Patent Application Publication EP 0875882 to Schiefer et al. (hereinafter "Schiefer").

B. Claims 9-11 are rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Schiefer in view of U.S. Patent Application No. 2003/0164897 to Chen et al. (hereinafter "Chen").

III. ARGUMENTS

On pages 10-17 in section (10) entitled "Response to Argument," the Examiner's Answer sets forth arguments in response to Appellant's Appeal Brief. Appellant responds to each of the Examiner's arguments below.

Independent claim 1 recites a ratio of two between the display frame rate and the source frame rate, as the single circular buffer allows at maximum, a ratio of 2 (1:2 or 2:1) between the respective frame rates to function properly without any video tearing. *See e.g., Figs. 5A-5E,* ¶¶ [0061]-[0063]. The adjustment includes three features: (1) a time offset between the two address pointers, (2) a fixed polarity of the pointers during the read period, and (3) a constant ratio between the display frame rate and the source frame rate (here, the ratio is equal to 2). *See* ¶ [0054]. As described in the specification in paragraph [0009], this subject matter relates to the use of a controller to control both the read and write address pointers in the memory that uses a single circular buffer in order to prevent video tearing. When the source and display frame rates are not equal, the controller adjusts both the frame rates and the address pointers so that, during the read period, one pointer does not cross the other, thus preventing tearing. *See* ¶ [0015], [0063].

In response to Appellant's argument that the clock rate cited in European Pub. No. EP0875882 to Schiefer et al. (hereinafter "*Schiefer*") is not equivalent to the frame rate in the claimed subject matter, on pages 12-13, the Examiner's Answer asserts that it would have been obvious to set a fractional frame rate given the fractional clock rate of *Schiefer*. However Appellant respectfully submits that

Schiefer's method differs and has a different principle of operation than the claimed subject matter.

Schiefer discloses a timing generator for format conversion of video. *See Schiefer at Abstract.* This system reformats video by synchronizing the output and input frame rates, using a memory buffer in case of errors to ensure a smooth display. The memory write controller controls write operations sequentially in a circular buffer sequence. *See id.,* at col. 13, lines 34-39. The data path, once full, is then controlled by a timing controller. The Examiner states that *Schiefer* discloses that "the output write clock is running at rate of four times the input clock rate in the example given." The statement in Examiner's Answer is a correct statement of fact, but the fact shows an error in the reasoning of the rejection. As the timing diagram of the clock rates indicates, *Schiefer* substantially differs in operation from the recited subject matter.

Schiefer scales and deinterlaces the input video and matches the frame rate of the input video with that of the output. The large ratio between input and output *clock rates* ("DCLK = 4*IPCLK", *see id. at* Fig. 11) disclosed by *Schiefer* and cited by the Examiner does not relate to the ratio between the input and output frame rates. Rather, the 4:1 ratio discussed in the *Schiefer* specification relates to the system horizontally and vertically upscaling an input *image* by a factor of 2 for an output video, while maintaining a locked, similar frame rate through the control of the respective *line rates* (*see id.,* at col. 21, lines 15-33 (discussing display line rate as a fractional multiple of the input video main clock)). These line rates differ due to the

respective number of pixels per line in the input and output images. *See id.*, at col. *21*, lines 34-46 (discussing means to force frame locking so the resulting display frame period is similar to the input video frame period.)

Schiefer, therefore, discloses a ratio for a clock rate, which is different from and not suggestive of the frame rate of the claimed subject matter. A person of ordinary skill in the art would not even be able to determine the frame rate when given only a clock rate.

Even assuming, *arguendo*, that a person of ordinary skill followed the teachings of *Schiefer*, the disclosed ratio of 4:1 between the respective address pointers in the singular buffer would guarantee video tearing stemming from an invalid ratio between frame rates, as one pointer with a rate four times faster than the other would always overtake the other pointer at some point in the circular buffer and would do so multiple times during a single traversal of the slower pointer through the circular buffer. For example, during a single 360-degree advance of the slower pointer, the faster pointer will overtake the slower pointer twice. In contrast, despite the mention in the claims of a ratio of 2, pointer overlapping does not occur in the recited subject matter because the ratio involves the display and source frame rates, and, as explained in paragraphs [0061]-[0063] and Figs. 5A-5E of the published version of the application, the maximum ratio which can be employed without the occurrence of pointer overlapping and video tearing. Accordingly, the clocks of *Schiefer* does not disclose or render obvious the recited

subject matter, at least because a person of skill in the art acting on any suggestion by *Schiefer* would not be led to the claimed subject matter.

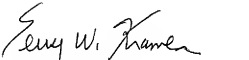
Moreover, it is respectfully submitted that a person of ordinary skill in the art would not even look to *Schiefer* as a reference here because said person would not be able to determine the frame rate with knowledge only of the clock rate. *Schiefer*, which discloses a solution for scaling a video image using a 4:1 clock ratio for line rates, has no connection to the recited subject matter, which has a maximum working limit of 2:1 between frame rates; a person of ordinary skill in the art following the suggestion by *Schiefer* of a 4:1 ratio would not be able to create the claimed subject matter. As such, *Schiefer* fails to disclose, teach, or suggest to a person of ordinary skill in the art all the elements recited in claims 1 and 2. *Schiefer* therefore does not render claims 1 and 2 obvious.

IV. CONCLUSION

For at least the reasons discussed above, it is respectfully submitted that the rejections are in error and that claims 1-11 are in condition for allowance. For at least the above reasons, Appellants respectfully request that this Honorable Board reverse the rejections of claims 1-11.

In the event that the fees submitted prove to be insufficient in connection with the filing of this paper, please charge our Deposit Account Number 50-0578 and please credit any excess fees to such Deposit Account. Should there be any remaining issues that could be readily addressed over the telephone; the Examiner is asked to contact the attorney overseeing the application file, David Schaeffer, of NXP Corporation at (408) 474-5256.

Respectfully submitted,
KRAMER & AMADO, P.C.



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